DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
NP70N10KUF

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

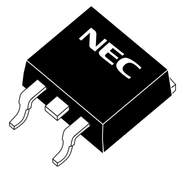
The NP70N10KUF is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP70N10KUF-E1-AZ Note	Pure Sn (Tin)	Tape	TO-263 (MP-25ZK)
NP70N10KUF-E2-AZ Note		800 p/reel	typ. 1.5 g

Note See “**TAPE INFORMATION**”

(TO-263)



FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
  $R_{DS(on)}$ = 20 mΩ MAX. (V_{GS} = 10 V, I_D = 35 A)
- Low C_{iss}: C_{iss} = 2500 pF TYP.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±70	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±135	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	1.8	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	120	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current Note2	I_{AS}	22	A
Single Avalanche Energy Note2	E_{AS}	48	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 50 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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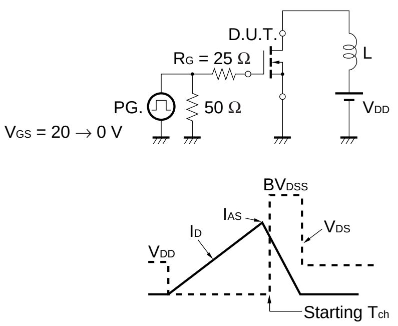
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

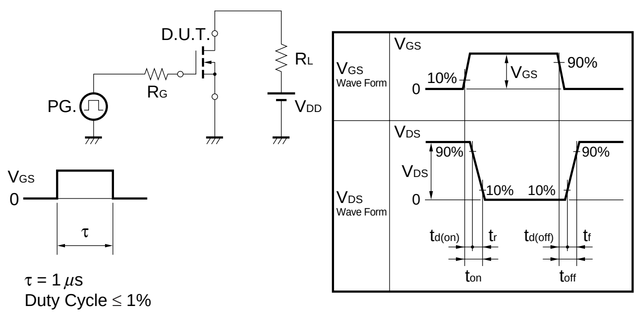
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250 μA, V_{GS} = 0 V	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.7	2.5	3.3	V
Forward Transfer Admittance Note	$\vert y_{fs} \vert$	V_{DS} = 10 V, I_D = 20 A	11	22		S
Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 35 A		17	20	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		2500	3750	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		270	410	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		110	200	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 35 A		25	53	ns
Rise Time	t_r	V_{GS} = 10 V		9	23	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		48	96	ns
Fall Time	t_f			7	18	ns
Total Gate Charge	Q_G	V_{DD} = 80 V		50	75	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		16		nC
Gate to Drain Charge	Q_{GD}	I_D = 70 A		19		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 70 A, V_{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 70 A, V_{GS} = 0 V		88		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		245		nC

Note Pulsed

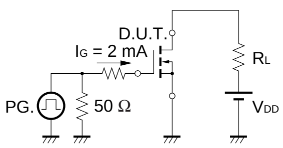
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

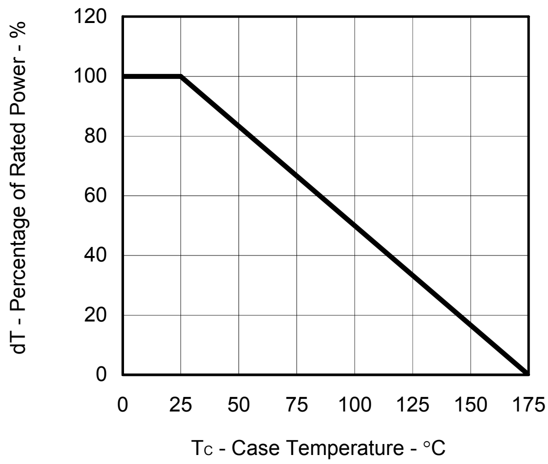


TEST CIRCUIT 3 GATE CHARGE

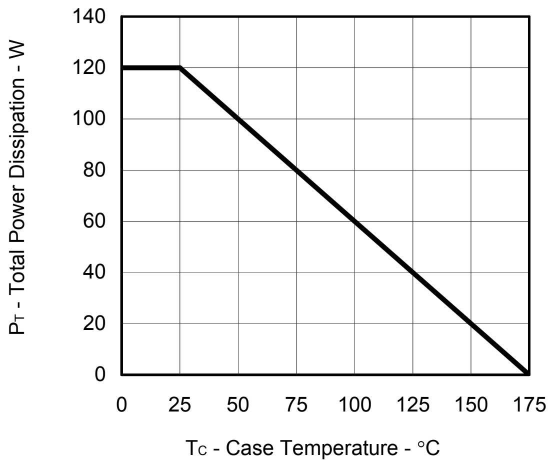


TYPICAL CHARACTERISTICS (T_A = 25°C)

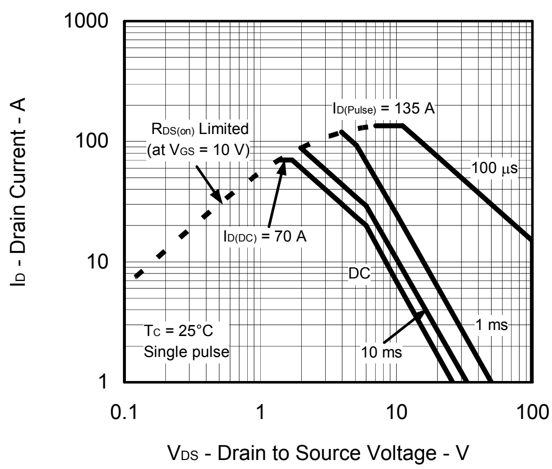
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



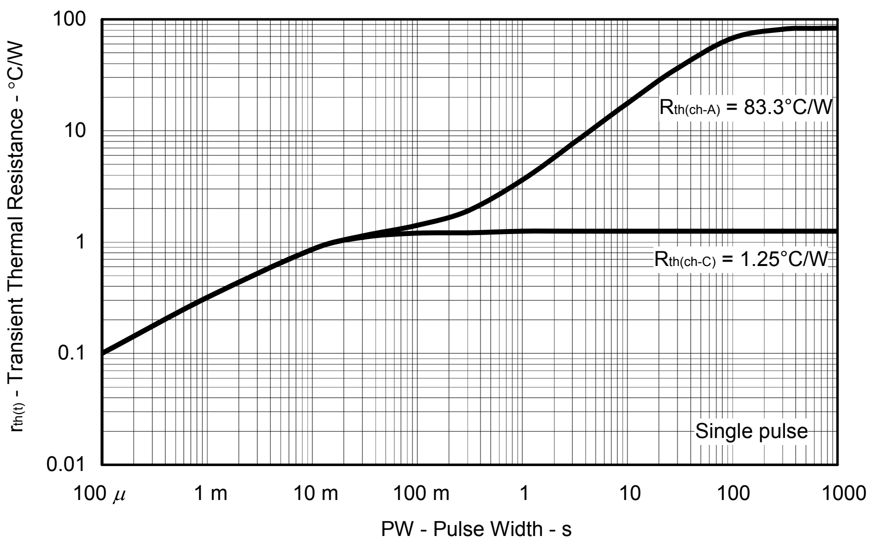
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



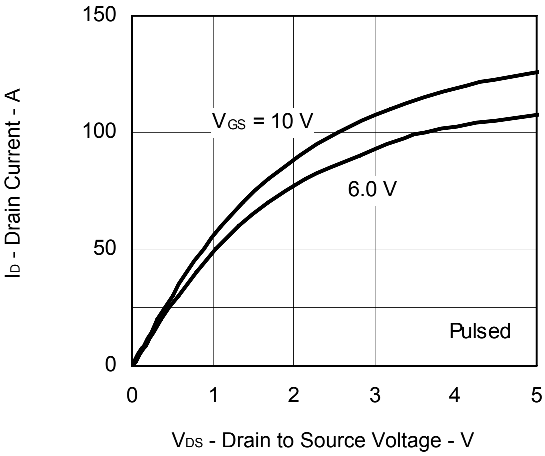
FORWARD BIAS SAFE OPERATING AREA



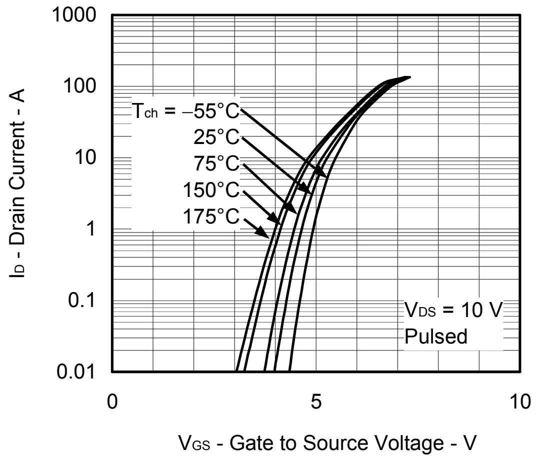
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



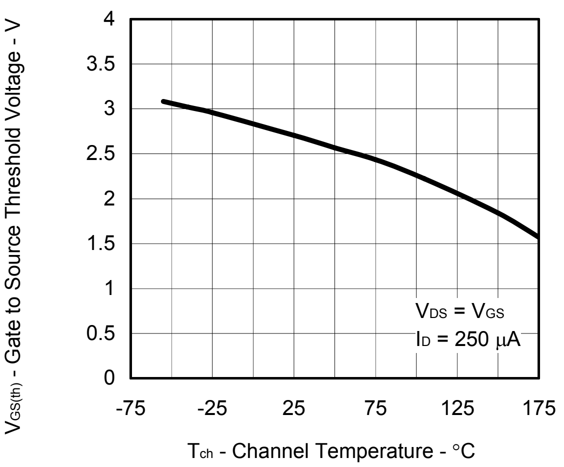
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



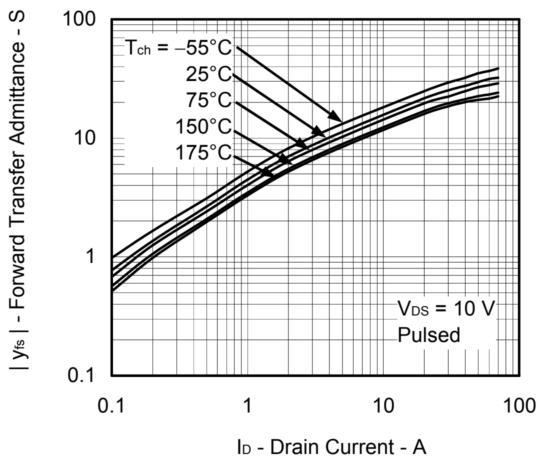
DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE



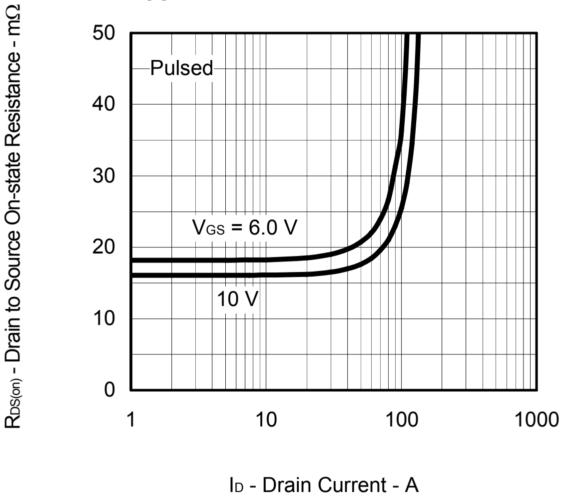
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



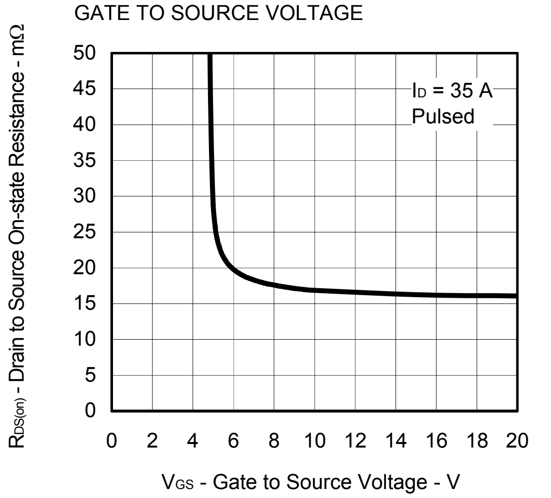
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



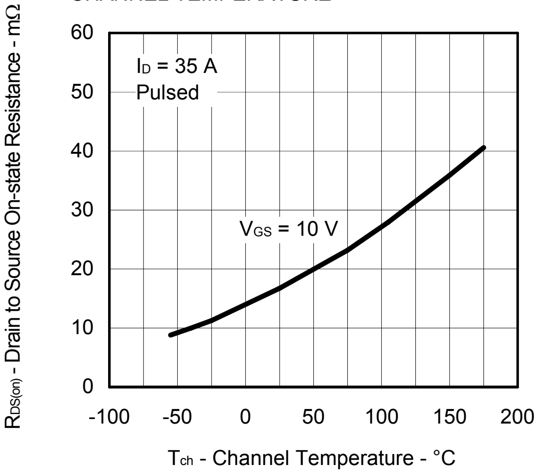
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



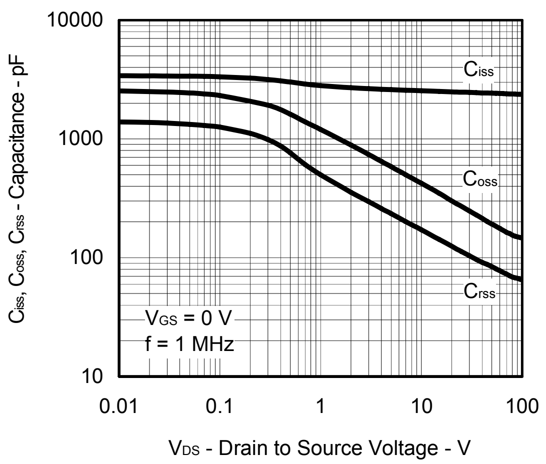
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



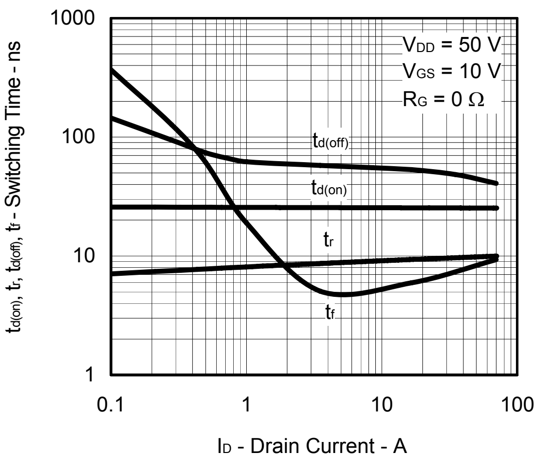
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



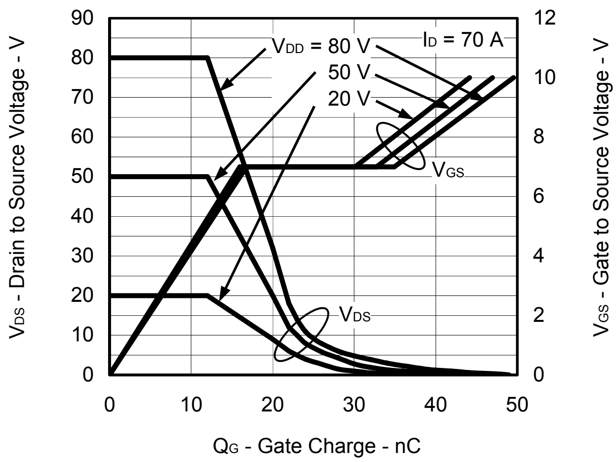
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



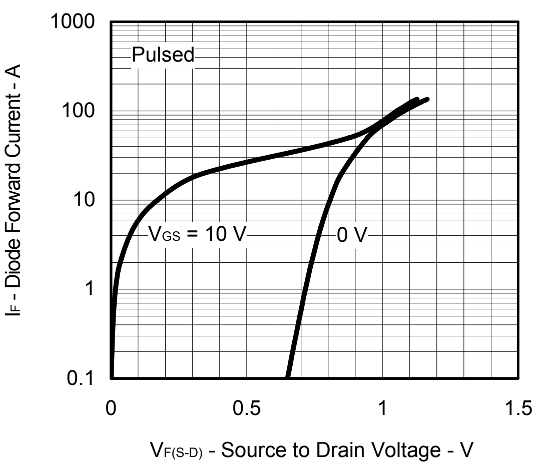
SWITCHING CHARACTERISTICS



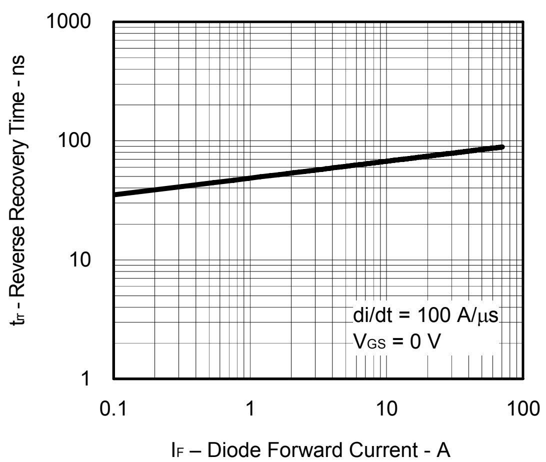
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



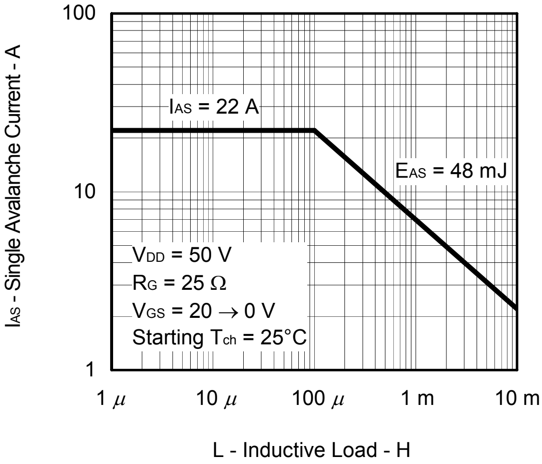
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



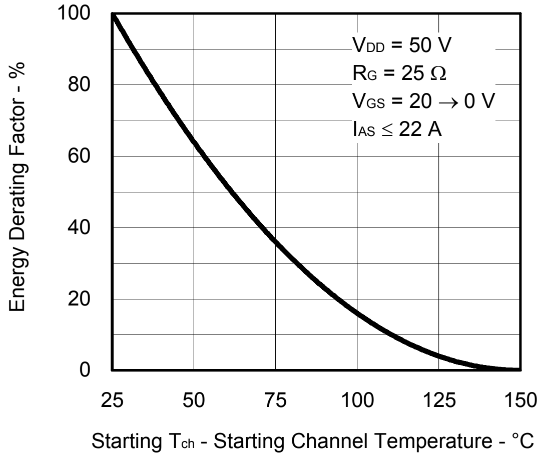
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

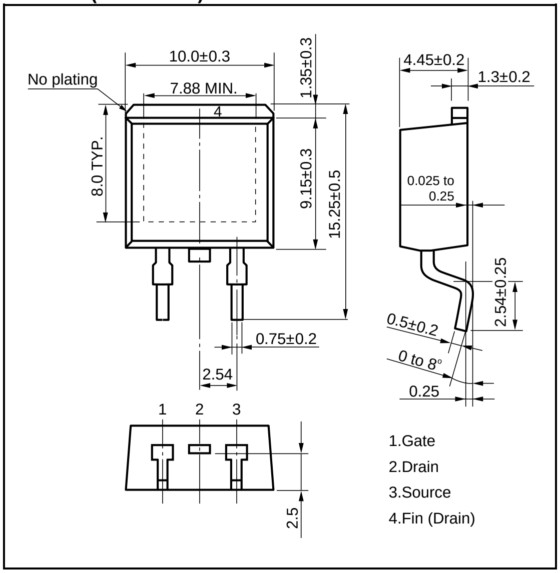


SINGLE AVALANCHE ENERGY DERATING FACTOR

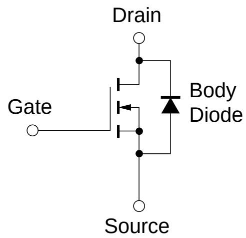


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT

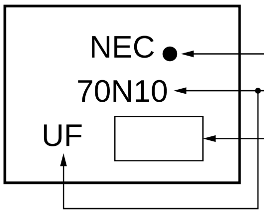


Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

<R> **TAPE INFORMATION**

There are two types (-E1, -E2) of taping depending on the direction of the device.

MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP70N10KUF should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).